ABSTRACT OF THE DISCLOSURE

In a level shift circuit, including two Nch transistors Tn1, Tn2 receiving a pair of complementary input signals and two Pch Transistors Tp1, Tp2 of which gate terminals are cross-coupled to each other, nodes A and B as the drains of the two Nch transistors Tn1, Tn2 operating in reverse to each other are connected together with a resistance Tp3. The resistance Tp3, constructed of a Pch transistor, is grounded at its gate to be in the normally ON state. For example, when the Nch transistors Tn1 and Tn2 go ON and OFF, respectively, a current initially flows from the high-potential node A through the resistance Tp3 to the low-potential node B, raising the potential at the low-potential node B. Thus, the potential rise at the node B is sped up compared with the case that only the Pch transistor Tp2 becoming ON contributes to the potential rise. This enables high-speed operation of the level shift circuit with a small number of elements.